Hall Ticket Number:

Code No. : 21605

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

M.E. (ECE: CBCS) I-Semester Main Examinations, January-2018

(Embedded Systems & VLSI Design)

Advanced Computer Organization

Time: **3** hours Max. Marks: **60**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

1. Draw the structure of IEEE 754 format for 32 bit floating point number.
2. List all the operations performed by a computer during the interrupt cycle.
3. Define addressing mode and what is the purpose of it?
4. What is the difference between a direct and indirect address instruction?
5. Write mapping procedures used for Cache organization.
6. Draw the block diagram of associative memory and explain.
7. Explain the strobe control method of asynchronous data transfer.
8. Define bus arbitration with reference to Direct Memory Access.
9. Compute the Instruction Issue Rate (IIR) and Instruction Issue Latency (IIL) of a super scalar super pipelined processor of degree (3, 5).
10. Give the idea behind dynamic scheduling.

Part-B (5 × 8 = 40 Marks)

11. a) Consider a non-pipelined processor with a clock rate of 2.5 GHz and average Cycles Per Instruction (CPI) of 4. The processor is upgraded to a pipeline processor with 5 stages, but due to internal pipeline delay issues, CPU clock speed is reduced to 2 GHz. Assume that there are no stalls in the pipeline. Analyze and estimate the speedup that can be achieved with these specifications. [4]

    b) Explain with examples the various hazards in pipelining. [4]

12. a) Hard-wired control unit is faster than micro programmed control unit. Justify this. [4]

    b) Distinguish between horizontal and vertical microinstruction. [4]

13. a) Explain, with the help of a diagram, virtual memory organization. [5]

    b) A computer system uses 3 level memory hierarchy with L1 cache, L2 cache and main memory. [3]

    Following are the specifications of the memory hierarchy.

    i) Block size in L1 cache is 4 words and L2 cache is 16 words.
    ii) Memory access times are 2 ns, 20 ns and 200 ns for L1 cache, L2 cache and main memory units respectively.
    iii) When there is a miss in L1 cache and a hit in L2 cache, a block of data is transferred from L2 cache to L1 cache unit.

    Analyze and evaluate the time required for transfer of one block of data from L2 cache to L1 cache unit. Assume any data, if missing.

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14. a) Define I/O interface. What are the functions of an I/O interface? [4]

    b) Describe the Peripheral Component Interconnect (PCI) Bus Standards. [4]

15. a) What is instruction-level parallelism? Explain in detail about various dependencies caused in ILP. [4]

    b) The time delays of 4-segments in the ALU pipeline are given below. [4]
    $t_1 = 40$ ns, $t_2 = 30$ ns, $t_1 = 100$ ns and $t_1 = 50$ ns.

    i) Compute the execution required to add 200 pairs of operands in the pipeline stages.

    ii) How do you reduce the execution time to 30% of the execution time calculated in part (i).

16. a) Describe how a processor executes instructions. Explain it with the help of a diagram. [4]

    b) With a neat block diagram, explain control unit organization. [4]

17. Answer any ***two*** of the following:

    a) Analyze and compare the performance parameters of super scalar, super pipelined and super scalar super pipelined processors. [4]

    b) Explain how USB support Isochronous data. [4]

    c) Describe the key characteristics and application areas of Vector processors. [4]